

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

D. RemarksRejection of Claims 1-3, 5-12, 14, and 16-20 Under 35 U.S.C. §102(b) based on U.S. Patent No. 5,981,353 (Tsai).

5 The rejection of claims 1-3 and 5-11 will first be addressed.

The invention of amended claim 1 is directed to a method that includes forming a first layer comprising silicon nitride over a first and second side of a substrate, and maintaining the second side of the substrate essentially free of any other overlying layers. The method further includes removing at least a portion of the first layer formed over the second side of the substrate, and forming device features on the first side of the substrate.

As is well known, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference. Because amended claim 1 includes limitations not shown in the cited reference, this ground of rejection is believed to be traversed.

15 *Tsai* is directed to a method of forming a shallow trench isolation region. The reference sets forth five particular examples. However, none of the examples is believed to show or suggest all of the limitations of amended claim 1.

The "Background of Invention" of *Tsai* discloses a manufacturing process of shallow trench isolation regions. This first example shows the simultaneous formation of a silicon nitride layers on a front surface of a wafer and a backside of the wafer (argued to correspond to Applicants' first layer on the second side of the substrate). However, in *Tsai*, the silicon nitride layer on the backside of the wafer is not maintained essentially free of other overlying layers. In particular, two process steps of this first example form and thicken another overlying layer of silicon oxide on the silicon nitride layer:

25 [A] side-wall oxide layer 104 is then grown on a surface of wafer 100 within the shallow trench 103. Concurrently, a silicon oxide layer 105 is formed over the backside of silicon nitride layer 102'.<sup>1</sup>

30 Next, a sealing operation is performed. Due to the heat generated and the oxygen

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<sup>1</sup> *Tsai*, Col. 2, Lines 5-8.

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

used during the sealing operation, the silicon oxide layer 105 at the backside of wafer 100 thickens.<sup>2</sup>

Accordingly, this first example of *Tsai* does not show “maintaining the first layer on the second side of the substrate essentially free of any other overlying layers”, as recited in amended claim 1.

The next two described examples of *Tsai* are based on the above first example, thus also do not include the above claim 1 limitation, either. In particular, the two examples are “based on the embodiment of FIG. 1d”, and thus form a silicon oxide layer on the bottom silicon nitride layer.<sup>3</sup>

The fourth example of *Tsai* shows “directional” formation of a silicon nitride layer, thus only forms a silicon nitride layer on a top surface of the wafer and not a bottom surface of the wafer:

[T]he silicon nitride layer 604 is only formed on the front of the wafer surface using the two methods mentioned above...<sup>4</sup>

Accordingly, this example cannot show “a first layer on a second side”, let alone a first layer on a second side that is maintained essentially free any other overlying layers, as recited in amended claim 1.

The last example of *Tsai* show the simultaneous formation of polysilicon layers on a front surface of a wafer and a backside of the wafer, thus cannot show or suggest Applicants’ first layer of silicon nitride.

Accordingly, because the cited reference does not show all the limitations of claim 1, this ground for rejection is traversed.

The rejection of claims 12 and 14 will now be addressed.

The invention of amended claim 12 is directed to a method that comprising various steps,

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<sup>2</sup> *Tsai*, Col. 2, Lines 13-16.

<sup>3</sup> See *Tsai*, Col. 4, Line 27 and Lines 42-43, as well as FIG. 1d, which shows overlying silicon oxide layer 105 formed on bottom silicon nitride layer 102’.

<sup>4</sup> *Tsai*, Col. 4, Line 67 to Col. 5, Line 2.

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

including forming a first layer that includes a first part formed over a first substrate side and a second part formed over a second substrate side. The method also includes forming a second layer over the first part while maintaining the second substrate side essentially free of any other additional layers, and removing at least a portion of the second part. The method further  
5 includes, after removing at least the portion of the second part, forming features on the first substrate side.

Applicants' amended claim 12 includes the limitation of "forming a second layer over the first part while maintaining the second substrate side essentially free of any other additional layers". As understood from the above discussion for claim 1, the first three examples of *Tsai*  
10 form a silicon nitride layer (argued to correspond to Applicants' second part) on the backside of a wafer. However, such examples have specific steps that form an additional overlying silicon oxide layer on this bottom silicon nitride layer. Consequently, these examples cannot show all the above limitations of claim 12.

It will be recalled that the fourth example of *Tsai* does not form a silicon nitride layer on the backside of the wafer, thus does not include a "second part" of a first layer, as recited in  
15 claim 12.

The last example of *Tsai* shows an arrangement in which a polysilicon layer is formed on the backside of a wafer. The figures of *Tsai* do not show the formation of any additional layers on this backside polysilicon layer. However, this example of *Tsai* forms features in the top  
20 surface of the wafer before removing the polysilicon layer<sup>5</sup>. Thus, this last example does not show "after removing at least the portion of the second part, forming features on the first substrate side", as set forth in amended claim 12.

For all of these reasons, the cited reference is not believed to show all the limitations of claim 12, and this ground for rejection is believed to be traversed.

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The rejection of claims 16-20 will now be addressed.

The invention of claim 16 is directed to a shallow trench isolation (STI) method. The STI method includes forming a trench etch mask layer over a first and second substrate side, the trench etch mask layer a layer silicon nitride deposited over the first and second substrate sides;

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<sup>5</sup> See *Tsai*, FIGS. 7a to 7c, which shows that bottom polysilicon layer 704' is removed only after dielectric layer 708 has been formed.

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

maintaining the trench etch mask layer over the second substrate side essentially free of any additional overlying layers; and removing at least a portion of the trench etch mask layer that is formed over the second substrate side.

To address this ground of rejection, Applicants' incorporate by reference herein the same  
5 general comments set forth for claim 1. Namely, that *Tsai* does not show or suggest the formation of a silicon nitride etch mask layer over a second substrate side that is maintained essentially free of any additional overlying layers. In particular, *Tsai* teaches a silicon nitride layer on the backside of the wafer on which is formed an additional overlying layer of silicon oxide.

10 Rejection of Claims 1-2, 8, 10-13 and 15 Under 35 U.S.C. §102(b) based on U.S. Patent No. 5,738,757 (*Burns et al.*).

The rejection of claims 1-2, 8 and 10-11 will first be addressed.

As noted above, Applicants' amended claim 1 recites a method that includes forming a  
15 first layer on a second side of a substrate, and maintaining the second side of the substrate essentially free of any other overlying layers.

*Burns et al.* teaches a multi-depth silicon etching method that forms silicon nitride layers on top and bottom surfaces of a silicon wafer. However, unlike Applicants' claim 1 invention, in *Burns et al.* the second side of the substrate is not maintained essentially free of other overlying  
20 layers. In particular, four layers are formed on the bottom surface of the wafer: two layers of silicon dioxide and two layers of silicon nitride<sup>6</sup>.

Accordingly, the cited reference is not believed to show all limitations of claim 1, and this ground of rejection is traversed.

25 The rejection of claims 12-13 and 15 will now be addressed.

As noted previously, amended claim 12 includes the limitation of "maintaining the second substrate side essentially free of any other additional layers". However, as discussed immediately above, in *Burns et al.* multiple additional layers are formed on the bottom of a wafer surface. Thus, all limitations of amended claim 12 are not shown by the cited reference.

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<sup>6</sup> See *Burns et al.*, which shows a bottom surface of silicon wafer 10 on which is formed silicon dioxide layer 12, silicon nitride layer 14, silicon oxide layer 16 and silicon nitride layer 18.

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**Rejection of Claim 4 Under 35 U.S.C. §103(a), based on *Tsai*.

As is well understood, to establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.

To the extent that this ground for rejection relies on *Tsai* to show various features of independent claim 1, the comments set forth above for claim 1 are incorporated by reference herein. Namely, the various examples of *Tsai* do not show or suggest all limitations of claim 1. Accordingly, all the limitations of claim 1 are not shown by the cited reference, and a prima facie case of obviousness has not been established.

In addition or alternatively, Applicants' claim 4 recites a particular silicon nitride thickness limitation of less than 3,000 angstroms. It is admitted that *Tsai* does not show such a limitation<sup>7</sup>.

To show Applicants' claim 4 limitations, the rejection proposes modifying *Tsai*:

It would have been desirable to form the Si<sub>3</sub>N<sub>4</sub> layers in the process taught above such that an adequate level of thickness is provided to properly construct the STI device without using an excessively thick layer of Si<sub>3</sub>N<sub>4</sub> which would undesirably waste process time, and undesirably increase process cost<sup>8</sup>.

Applicants note that this proposed suggestion/motivation does not appear to originate from any the cited references, and provides no motivation for Applicants' specific numerical limitation of 3,000 Å. Accordingly, Applicants seasonably traverse the above statement and request the citation of references in support.

Accordingly, because all limitations of claim 4 are not shown or suggested by the cited reference, and the requisite suggestion/motivation for the proposed modification is believed to be lacking, this ground for rejection is traversed.

<sup>7</sup> See the Office Action, dated 9/9/03, Page 4, Lines 17-18.

<sup>8</sup> See the Office Action, dated 9/9/03, Page 4, Lines 21-24.

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE****Rejection of Claims 3-5 Under 35 U.S.C. §103(a), based on *Burns et al.***

To the extent that this ground for rejection relies on *Burns et al.* to show various features of independent claim 1, the comments set forth above for claim 1 are incorporated by reference herein. Namely, that *Burns et al.* does not show or suggest all limitations of claim 1.  
5 Accordingly, all the limitations of claim 1 are not shown by the cited reference, and a prima facie case of obviousness has not been established for these claims.

In addition or alternatively, to address the rejection of claim 4, Applicants incorporate by reference the same general comments set forth above for the rejection of claim 4 based on *Tsai*. That is, it is admitted that *Burns et al.* does not show the limitations of claim 4<sup>9</sup>, and the  
10 proposed suggestion/motivation for modifying *Burns et al.* does not appear to originate from any the cited references, and provides no motivation for Applicants' specific numerical limitation of 3,000 Å. Accordingly, Applicants also seasonably traverse the statements relied upon for this ground of rejection, and request the citation of references in support.

For all of these reasons, this ground for rejection is traversed.

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Claims 1, 12 and 16 have been amended. Claims 3-4, 11 and 19 have also been amended, not in response to the cited art, but to change claim dependencies in response to cancelled claims, and further clarify features of the invention. Claims 2 and 17 have been cancelled.

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<sup>9</sup> See the Office Action, dated 9/9/03, Page 4, Lines 17-18.

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

The present claims 1, 3-16 and 18-20 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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